



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Surjit Talwar et al.

Title: LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT

Docket No.: 1365.063US1

Serial No.: 10/714408

Filed: November 14, 2003

Due Date: N/A

Examiner: Unknown

Group Art Unit: 2124

**MS Non-Fee Amendment**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

☒ A return postcard.

☒ A Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.), and copies of 7 cited documents.

If not provided for in a separate paper filed herewith, Please consider this a **PETITION FOR EXTENSION OF TIME** for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

Customer Number 21186

By: 

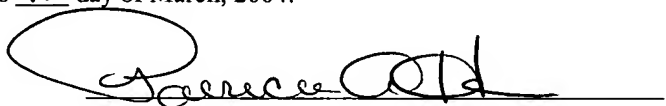
Atty: Timothy B. Clise

Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 9<sup>th</sup> day of March, 2004.

PATRICIA A. HULTMAN

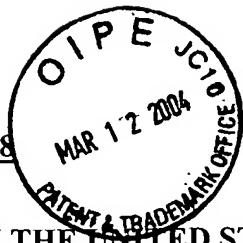
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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

(GENERAL)

S/N 10/714,408



PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant:	Sunil Talwar et al.	Examiner:	Unknown
Serial No.:	10/714,408	Group Art Unit:	2124
Filed:	November 14, 2003	Docket:	1365.063US1
Title:	LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT		

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**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Supplemental Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Supplemental Information Disclosure Statement considered.

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Serial No :10/714408

Filing Date: November 14, 2003

Title: LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT

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The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

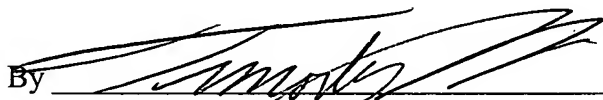
Respectfully submitted,

SUNIL TALWAR ET AL.

By their Representatives,


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Date 9 March '04

By   
Timothy B Clise  
Reg. No. 40,957

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Name

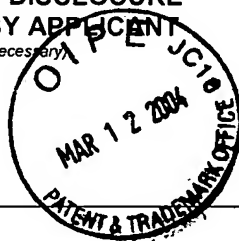
  
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)



Complete if Known

Application Number 10/714408

Filing Date November 14, 2003

First Named Inventor Talwar, Sunil

Group Art Unit 2124

Examiner Name Unknown

Sheet 1 of 1

Attorney Docket No: 1365.063US1

**US PATENT DOCUMENTS**

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
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**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T <sup>2</sup>
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**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		BEDRIJ, O. J., "Carry-Select Adder", <u>IRE Trans., EC-11</u> , (June 1962), 340-346	
		KNOWLES, S., "A Family of Adders", <u>Proc. 14th IEEE Symp. on Computer Arithmetic</u> , (1999), 30-34	
		KOGGE, P. M., et al., "A Parallel Algorithm for the Efficient Solution of a General Class of Recurrence Equations", <u>IEEE Trans. Computers</u> , Vol. C-22, No. 8, (Aug. 1973), 786-793	
		LADNER, RICHARD E., et al., "Parallel Prefix Computation", <u>Journal of ACM</u> , Vol. 27, No. 4, (Oct. 1980), 831-838	
		LING, HUEY, "High-Speed Binary Adder", <u>IBM Journal of Research and Development</u> , Vol. 25, No. 3, (1981), 156-166	
		SKLANSKY, J., "Conditional-Sum Addition Logic", <u>IRE Trans., EC-9</u> , (June 1960), 226-231	
		WEINBERGER, A., et al., "A Logic for High-Speed Addition", <u>Nat. Bur. Stand. Circ., 591</u> , (1958), 3-12	

**EXAMINER****DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached